MICROMACHINED STIMULATING MICROELECTRODE ARRAYS

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MICROMACHINED STIMULATING MICROELECTRODE ARRAYS

Summary

This contract seeks to develop a family of thin-film stimulating arrays for use in neural prostheses. STIM-2B/-3B are two- and three-dimensional arrays of stimulating sites on 400µm centers. The probes have four channels and 64-sites. Any selected site can be used for either recording or stimulation. Current generation is off-chip. The high-end probes STIM-2/-3 are similar except they use on-chip current generation via 8-bit digital to analog converters.

During the past quarter, work under this program focused in two areas: completion of the design of our high-end stimulating probes, STIM-2 and STIM-3, and completion of the design of a wireless interface for use with the probes. Both of these were completed and both the probes and the interface are in fabrication.

The STIM-2 and STIM-3 probes are designed to provide 64 sites and 8 parallel channels per probe. The are designed for fabrication in the U-M 3µm micromachined p-well double-poly single-metal CMOS process and operate from ±5V supplies using seven input leads. A platform chip with a layout area of about 1.1mm by 2.7mm has also been completed to allow addressing of single probes in a multi-probe 3D array. The probes produce stimulating currents over a range from –127µA to +127µA with a current resolution of ±1µA. The circuit area measures 5.8mm wide by 2.5mm wide and is designed to lay flat against the cortex to minimize vertical height of the implant. The 90° fold-over with respect to the penetrating shanks is facilitated using silicon ribbon cables. The probe offers eight shanks on 400µm centers with eight sites per shank on 200µm centers. Any site on the probe can be used for recording using an on-chip recording amplifier having a midband gain of 40dB, a bandwidth from 3.2Hz to 14kHz, a power dissipation of 212µW, and an input-referred noise of 7.9µV/rt-Hz.

A wireless interface for use with the probes has also been developed. Many aspects of this chip have been reported previously. The complete design is now in fabrication using the U-M CMOS process. The wireless chip will be platform-mounted, and we hope to demonstrate fully-wireless operation of the stimulating system before the end of the year.

MICROMACHINED STIMULATING MICROELECTRODE ARRAYS

1. Introduction

The goal of this contract is the development of active multi-channel arrays of stimulating electrodes suitable for studies of neural information processing at the cellular level and for a variety of closed-loop neural prostheses. The probes should be able to enter neural tissue with minimal disturbance to the neural networks there and deliver highly-controlled (spatially and temporally) charge waveforms to the tissue on a chronic basis. The probes consist of several thin-film conductors supported on a micromachined silicon substrate and insulated from it and from the surrounding electrolyte by silicon dioxide and silicon nitride dielectric films. The stimulating sites are activated iridium, defined photolithographically using a lift-off process. Passive probes having a variety of site sizes and shank configurations have been fabricated successfully in past contracts and have been distributed to a number of research organizations nationally for evaluation in many different research preparations. For chronic use, the biggest problem associated with these passive stimulating probes concerns their leads, which must interface the probe to the outside world. Even using silicon-substrate ribbon cables, the number of allowable interconnects is necessarily limited, and yet a great many stimulating sites are ultimately desirable in order to achieve high spatial localization of the stimulus currents.

The integration of signal processing electronics on the rear of the probe substrate (creating an "active" probe) allows the use of serial digital input data that can be de-multiplexed on the probe to provide access to a large number of stimulating sites from a very few leads. Our goal in this area is to develop a family of active probes capable of chronic implantation in tissue. For such probes, the digital input data must be translated on the probe into per-channel current amplitudes that are then applied to tissue through the sites. Such probes generally require five external leads, virtually independent of the number of sites used. As discussed in previous reports, we have designed a series of active probes containing CMOS signal processing electronics. Two of these probes have been completed and are designated as STIM-1A and STIM-1B. A third probe, STIM-2, is now beginning a final iteration and is a second-generation version of our original high-end first-generation design, STIM-1. All three probes provide 8-bit resolution in digitally setting the per-channel current amplitudes. STIM-1A and -1B offer a biphasic range using $\pm5V$ supplies from $0\mu A$ to $\pm254\mu A$ with a resolution of $2\mu A$, while STIM-2 has a range from 0 to $\pm127\mu A$ with a resolution of $1\mu A$. STIM-2 offers the ability to select 8 of 64 electrode sites and to drive these sites independently and in parallel, while STIM-1A allows only 2 of 16 sites to be active at a time (bipolar operation). STIM-IB is a monopolar probe, which allows the user to guide an externally-provided current to any one of 16 sites as selected by the digital input address. The high-end STIM-2 contains provisions for numerous safety checks and for features such as remote impedance testing in addition to its normal operating modes. It also offers the option of being able to record from any one of the selected sites in addition to stimulation. It will be the backbone of a

multi-probe three-dimensional (3D) 1024-site array (STIM-3) now in development. A new probe, STIM-2B, has recently been added to this set. It offers 64-site capability with off-chip generation of the stimulus currents for four separate channels. These channels are organized in four groups so that each current can be directed to any of the 16 sites in its group. Each selected channel can be programmed for either stimulation or recording. On-chip recording amplifiers offer a gain of 50; alternatively, the neural activity can be recorded using off-chip amplifiers interfaced through the normal stimulating channels. This probe is available in both 2D and 3D versions (as STIM-2B/3B) and is now being used in-vivo.

During the past quarter, we have completed design and layout for both the high-end STIM-2 and STIM-3 probes and for a wireless interface for use with them. Both the probes and the wireless interface are now in fabrication. The results in these areas are described more fully in the sections below.

2. STIM-2/3: A Multiplexed Stimulating Probe with On-Chip Current Generation

During the past quarter, the redesigned STIM-2 and its 3-D version, STIM-3, have been laid out together with the platform addressing chip for STIM-3. The layout for STIM-2 is shown in Fig. 1. Its geometrical dimensions and electrical parameters are summarized in Table 1.

The redesigned STIM-2 features a new communication protocol with the external interface, an improved cascode current DAC, and a variety of test capabilities. Limited by the 3μm feature size, the circuit area is relatively large as shown in Table 1, which leads to a bulky probe structure. This should improve with reductions in the feature size and, especially, the development multi-metal-layer interconnections. The impact of a two-level metal system is being evaluated. The new capacitively-coupled amplifier designed for the recording probes has been employed here on the stimulating probe to achieve simultaneous stimulation and recording capability, with the amplifier modified to achieve compatibility with the larger power supplies used for the stimulation probes (±5V as opposed to ±1.5V for the recording probes). The schematic of the amplifier is shown in Fig. 2, and its simulation results are listed in Table 2. The AC frequency response is shown in Fig. 3.

The 3-D chronic version, STIM-3 is shown in Fig. 4. The back-end chip will be folded down via the silicon cables, which provide dielectric isolation for the interconnect but are difficult to fold at right angles, limiting the overall height of the stacked probes on platform. Alternative folding structures and configurations are also under development.
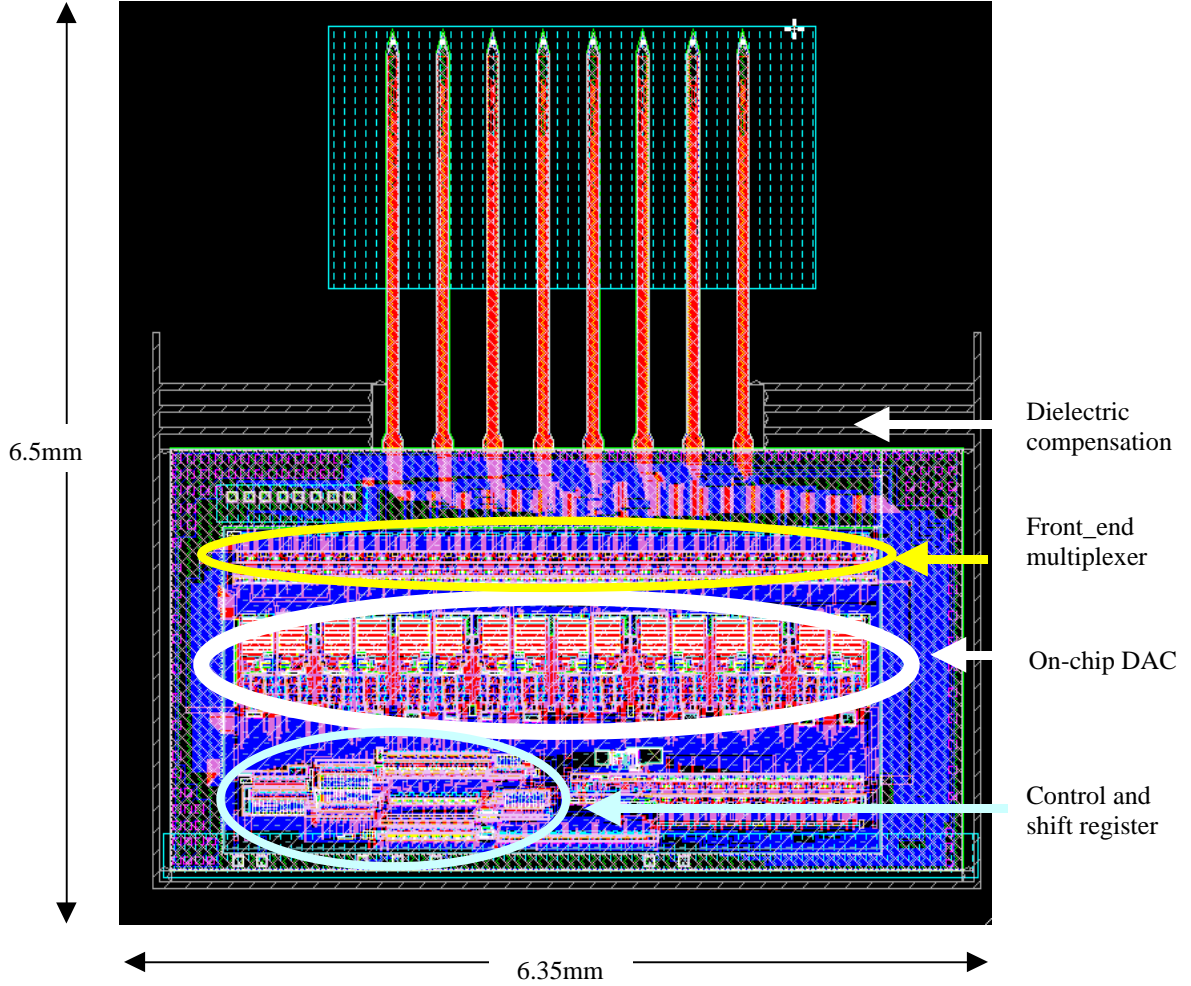
Fig. 1: Layout of STIM-2

Seven beam leads are gold-plated on the wings of STIM-3 to provide connections between the probe and platform. Among the seven leads, only the STB signal needs to be processed by the platform addressing circuit and then fed to the different probes on the platform. The other signals are directly passed from the probes to the external world. The timing diagram of the STB signals is shown in Fig. 5. The external signal processing circuitry delivers an STB strobe signal every 8 clock cycles. When the platform chip detects the platform addressing mode, the input probe address is decoded. In the specific case shown in Fig. 5, the first command is an extended mode for probe 1; thus, the STB line for probe 1 receives the strobe signals while the STB leads of other probes are tied to ground. After the first command finishes, the chip detects another platform address. This time the command is a simple mode for probe 2, so strobe signals are transmitted to the STB line in probe 2 and the STB leads of other probe are tied to ground. It is noted that there are two strobe signals at the end of operation for probe 1 before the platform chip forces it to ground; however, they cause no additional operations on probe 1. The layout of platform addressing chip is shown in Fig. 6. It controls the timing of the STB

signals it sends to different probes as shown in Fig. 5. The chip can be bonded to the platform and integrated with the telemetry circuitry.

Table 1. Specifications for STIM-2

Process technology	Bulk micromachined 3um n-epi, p-substrate, p-well CMOS process
Power supplies	Vcc=5V, Vss=-5V, GND=0V
Current range	±127 µA with 1uA resolution
Total chip area	5.8mm * 2.5mm
Total external leads	7 (Vcc, Vss, GND, Clock, Data_in, Data_out, STB)
Shank dimension	104µm (Width) , 3.3mm(Length)
Shank spacing	400µm
No. of shank	8
No. of sites per shank	8
Site area	1000µm^2
Site spacing	200µm

Table 2: Simulation results for the amplifier specification

Gain	40dB
Bandwidth	3.2Hz~14kHz
Power consumption	212.1µW
Input reference noise	7.93µVrms/⊠Hz
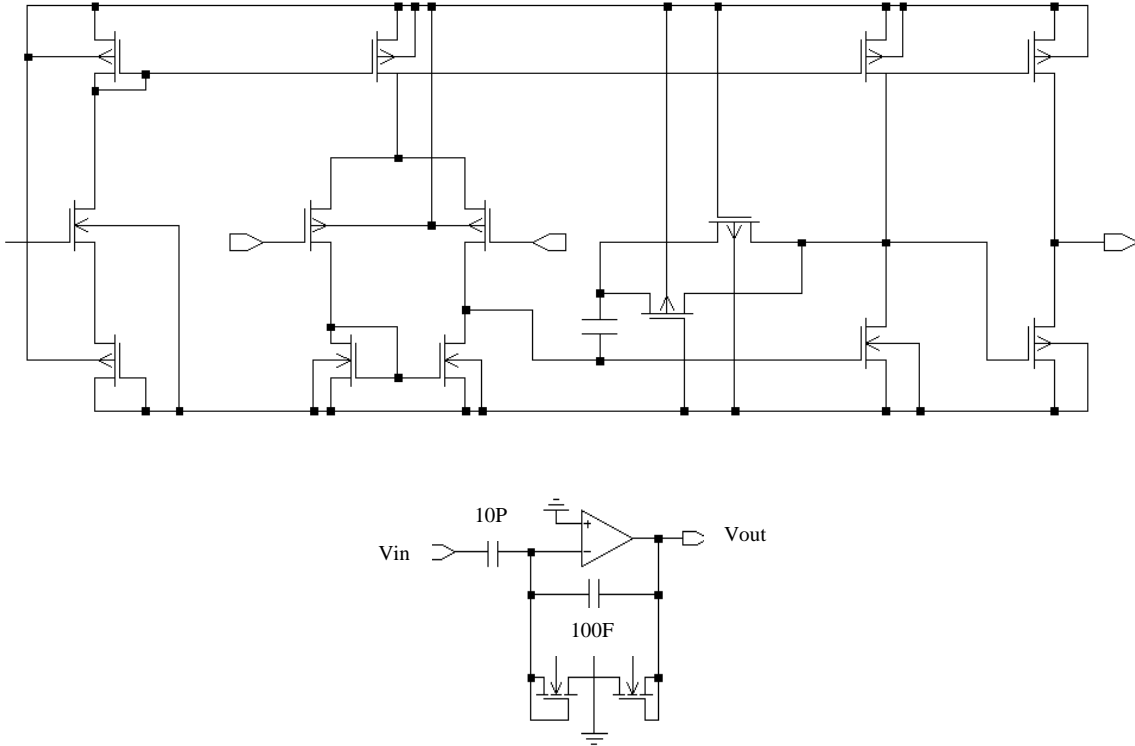
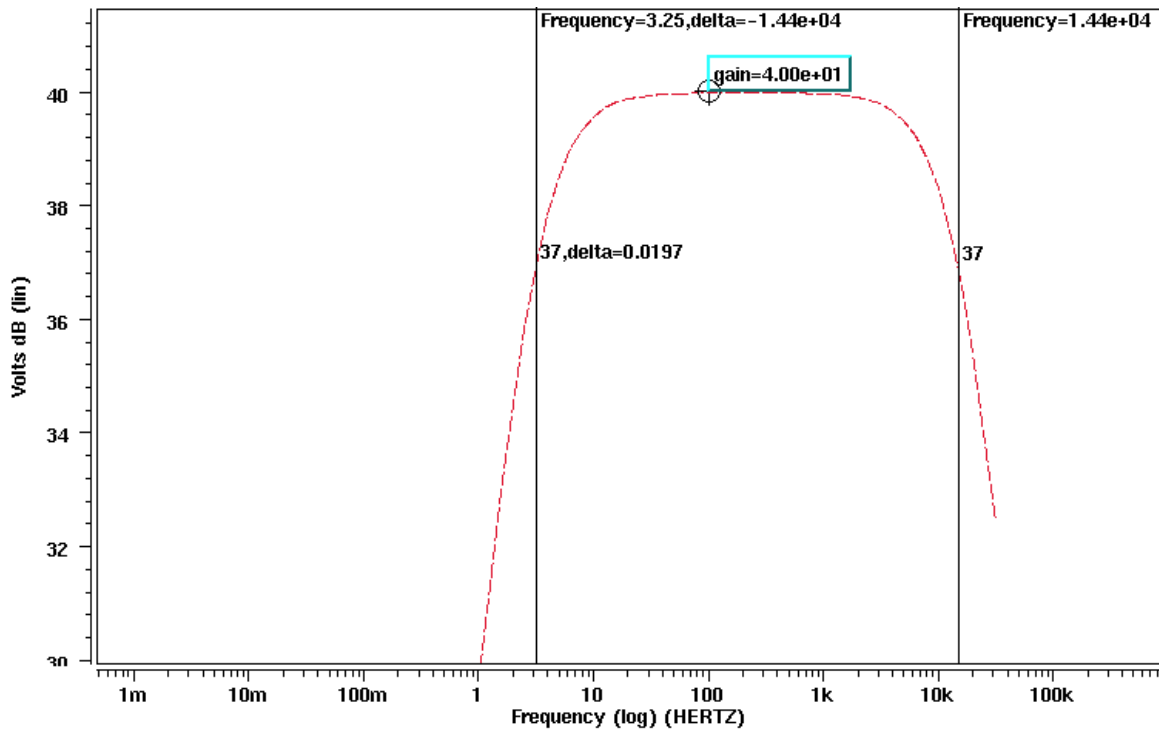Fig. 2: Schematic of the amplifier and its feedback configuration

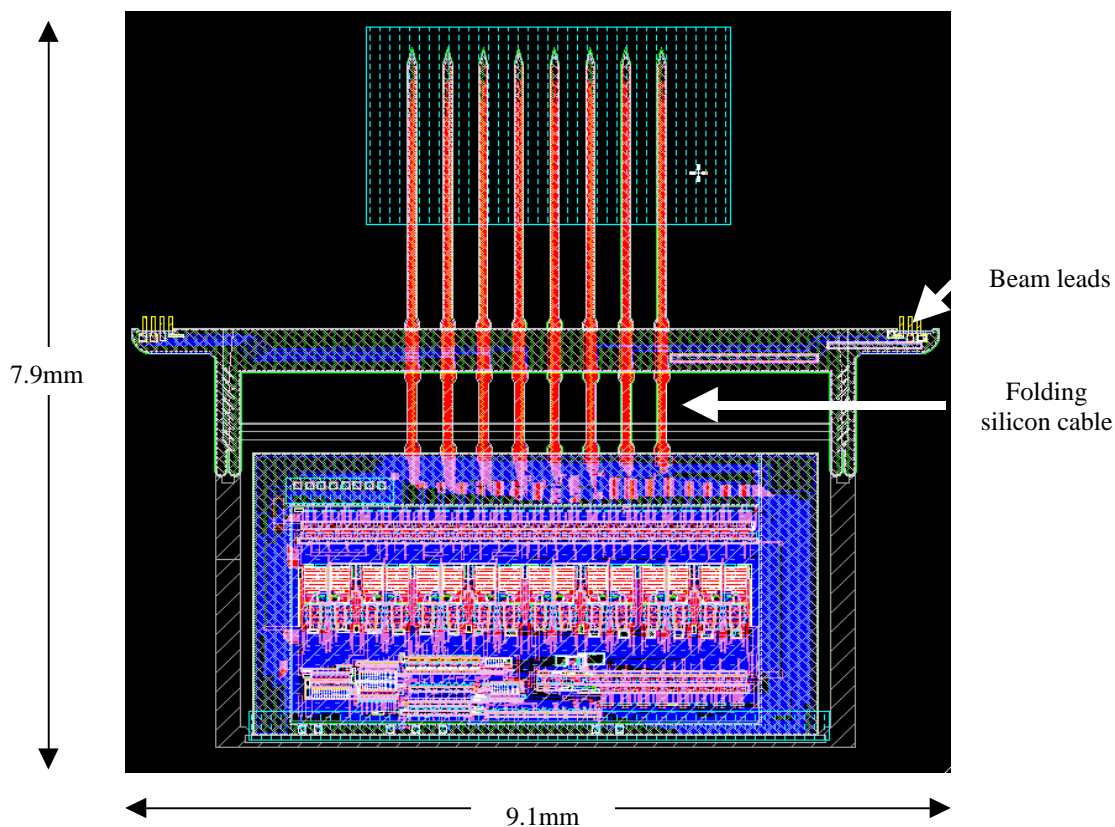Fig. 3: Output frequency response of the amplifier
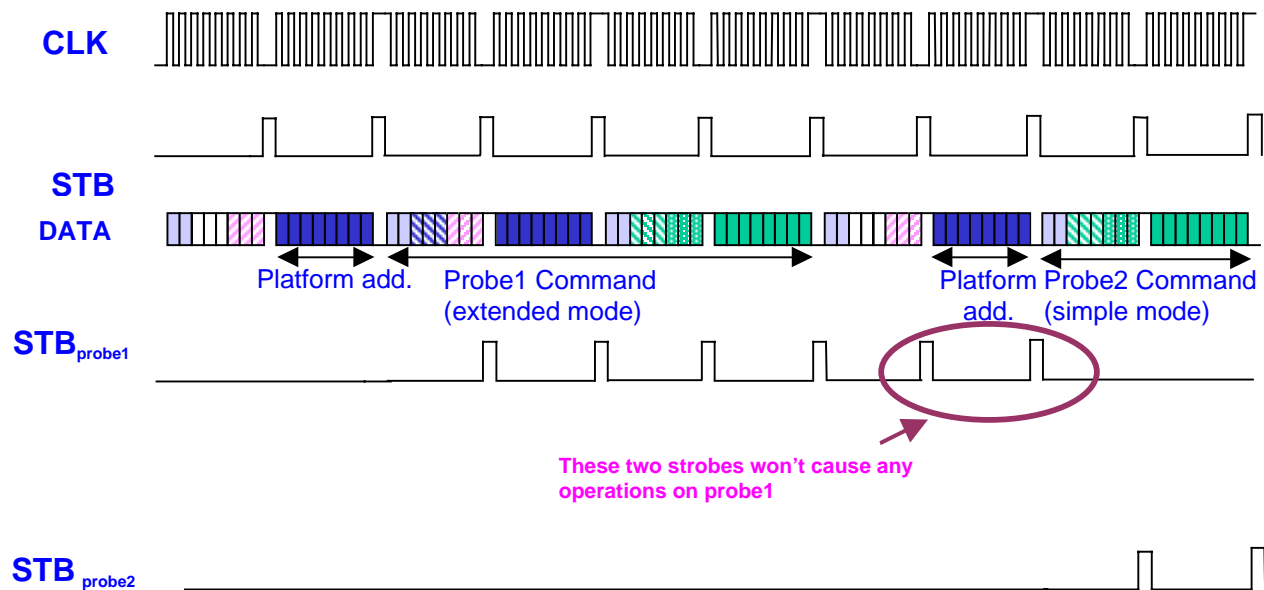
Fig. 4: Layout for STIM-3

Fig. 5: Timing diagram for the platform addressing circuitry

These probes and circuitry will be fabricated during the coming quarter. They will then be tested and compared to the simulation results. In the mean time, we will work on the 3-D fold-down structure to minimize the probe profile.
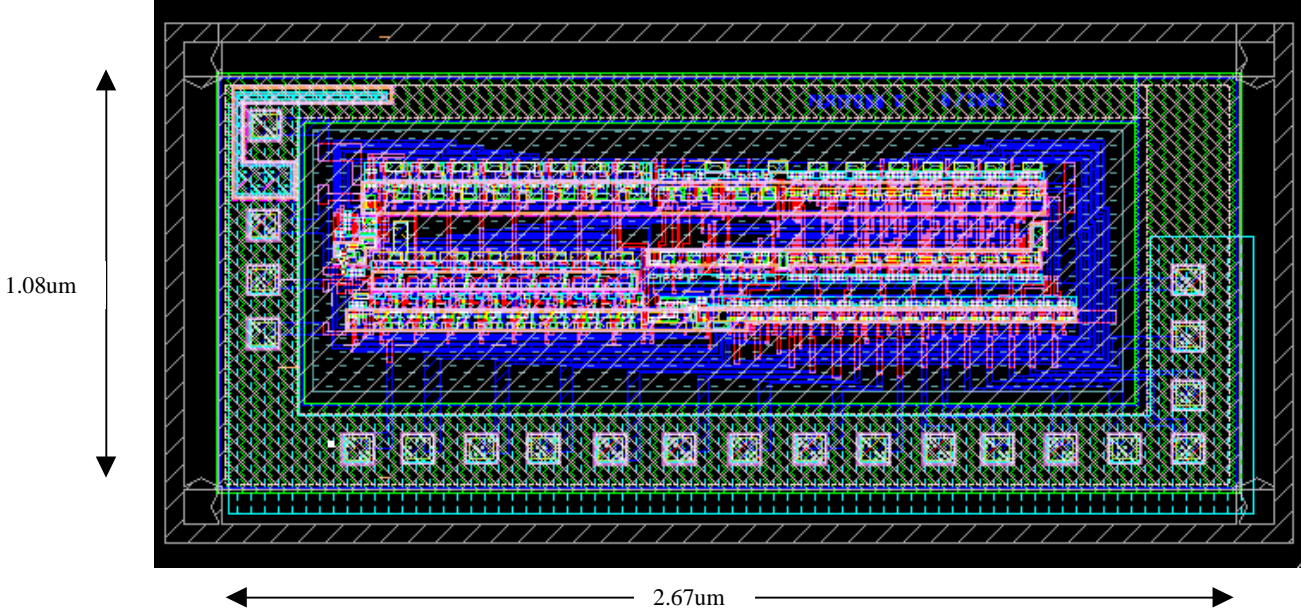

Fig. 6: Layout for platform addressing chip

3.   A Wireless CNS Stimulating System

The Complete Telemetry Interface Chip

The individual blocks of the telemetry interface chip for the wireless CNS stimulating system (INTERESTIM1) had been designed, fabricated, and tested during previous quarters. During this past quarter, all the blocks were put together and the complete interface chip was simulated and laid out. Some additional simulations, including parasitic effects, were done during the layout process and the designs were fine tuned for the next round of the U-M 3μm BiCMOS fabrication process, which is expected to begin in August. Three versions of the interface chip have been included on this run in addition to several test chips and new blocks to be added to the wireless CNS stimulating system in later runs.   Figure 7 shows the block diagram of the telemetry interface.
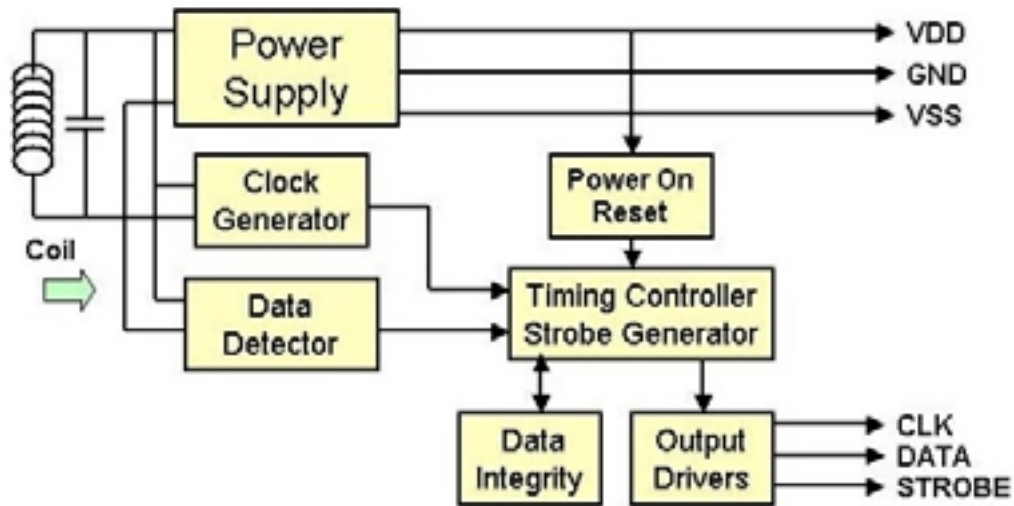
Telemetry Interface Block Diagram

Fig. 7: Block diagram of the first version of the telemetry interface chip, INTERESTIM1

Timing Controller and Strobe Generator

The timing controller and strobe generator block is the major digital part of the interface chip (INTERESTIM1). This block is designed compatible with the new STIM-2, which uses a separate strobe line with positive pulses as shown in Fig. 8.
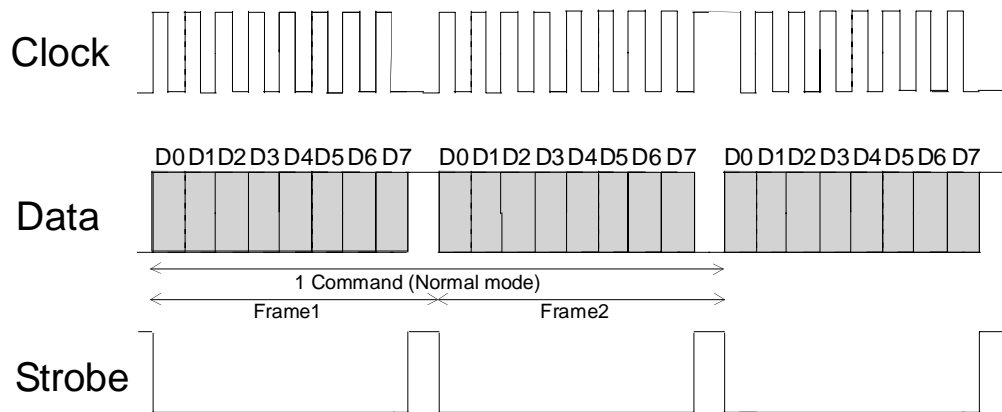

Fig. 8: The new STIM2 timing diagram

To generate the above signals, the timing block divides the regenerated clock, which is at the carrier frequency, with a selectable value to synchronize it with data detector baud rate. This stepped down clock (clkin) is then fed to the rest of the timing controller and strobe generator block along with the demodulated data as shown in Fig. 9.

Each command in the normal mode consists of two 1-byte frames. The strobe signal is generated at the 9th and 18th clock cycles. The first and the second frames are discriminated by forcing *Data=High* and *Clock=Low* at the 9th clock cycle (by the end of the first frame), and *Data=Low* and *Clock=high* at the 18th clock cycle (by the end of the second frame). The digital simulator showed no problems at this stage, but by taking a closer look at the waveforms after layout and parameter extraction, using the Accusim analog simulator, glitches and fake pulses were observed on the strobe and clock output signals. This can be seen on the 3rd and 4th traces in Fig. 10. The source of this problem was traced back to the differences in signal delays in several different paths to the outputs. This is primarily seen between the two paths that generate clock_out in Fig. 9. One of them directly comes from clkin while the other one passes through a 5-bit timer and its logic, which generate the n8_ and n17_ signals. In order to eliminate this problem, delay blocks were added in the clkin direct path to the output; the resulting waveform was free of glitches and extra clock pulses as is shown in Fig. 11. The digital block layout was then revised by adding delay elements and is shown in Fig. 12.
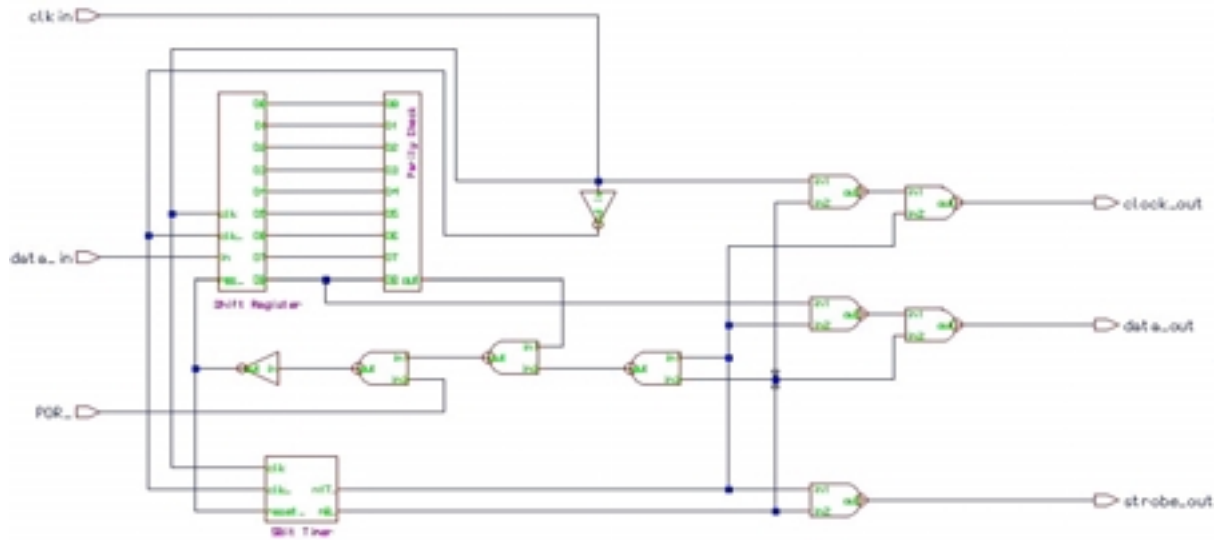

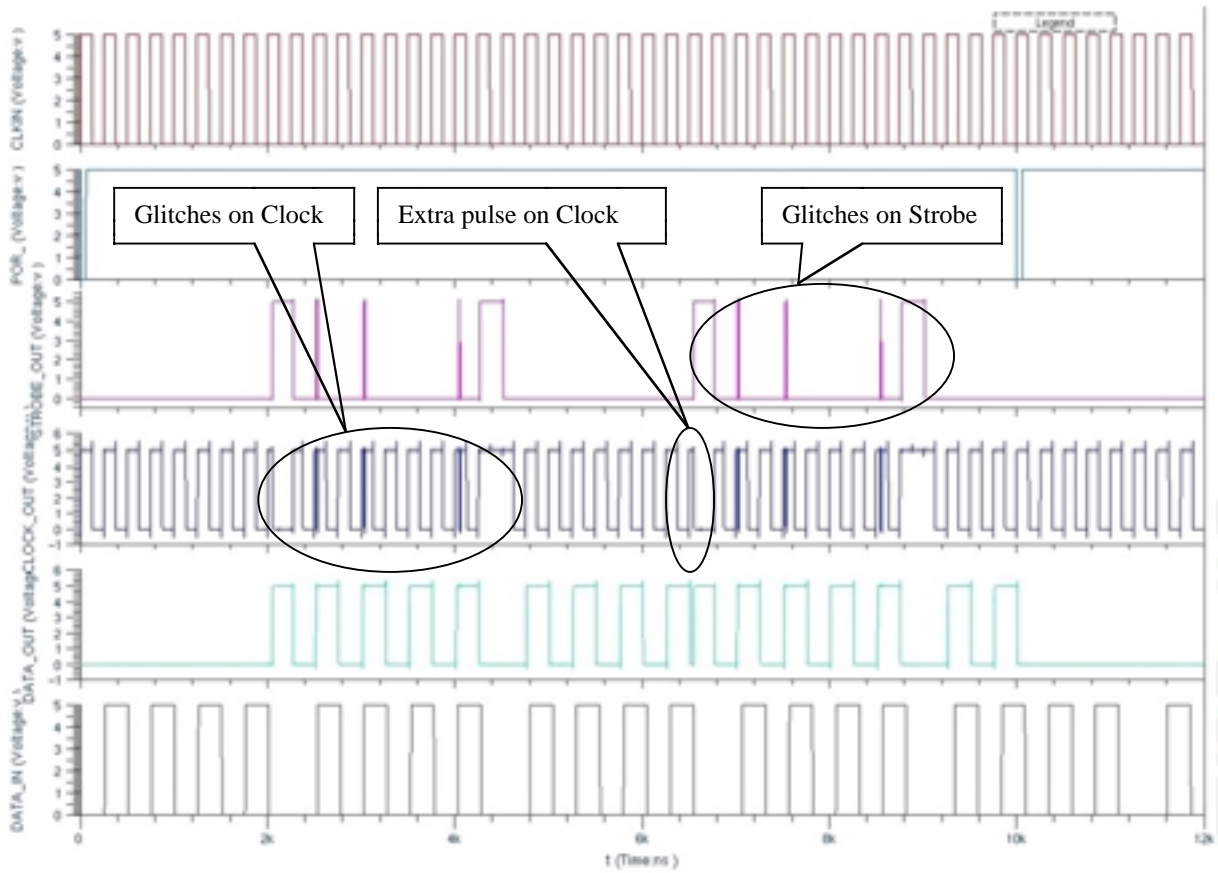Fig. 9: The high-end part of timing controller and strobe generator block.

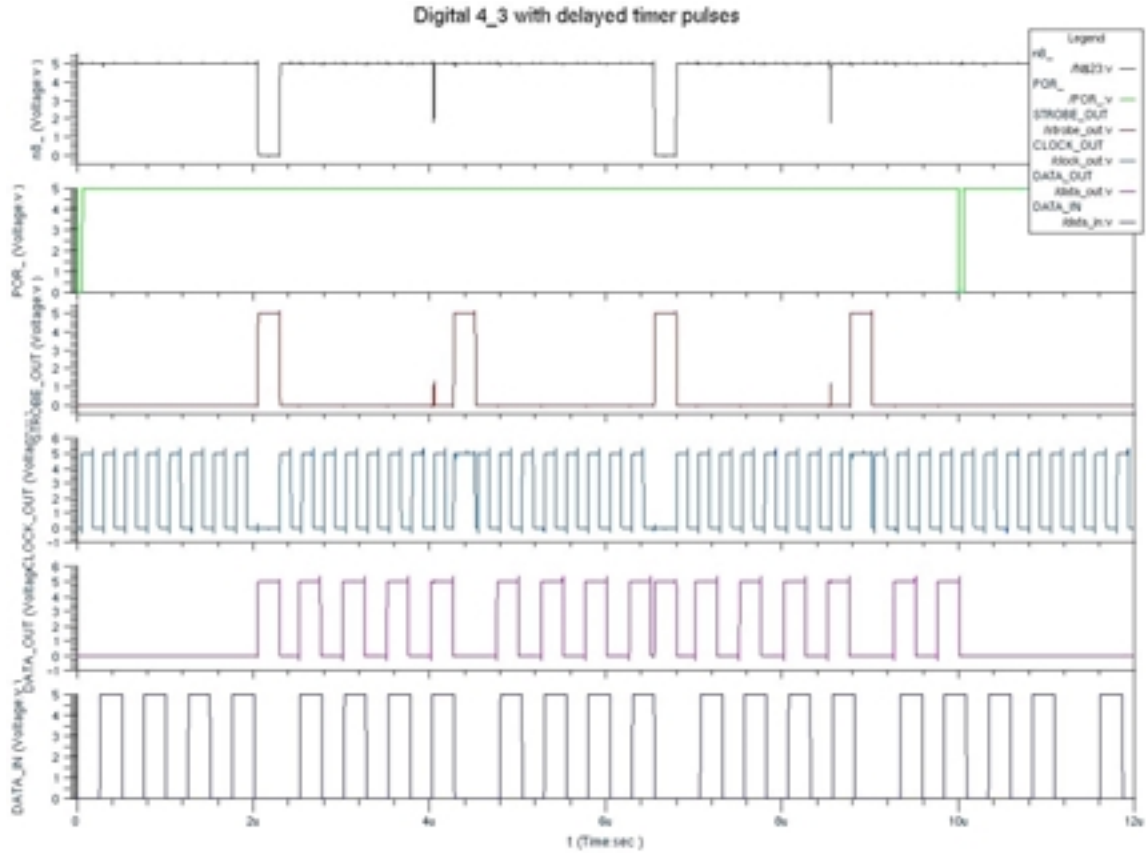Fig. 10: Glitches and fake pulses on the digital output waveforms.

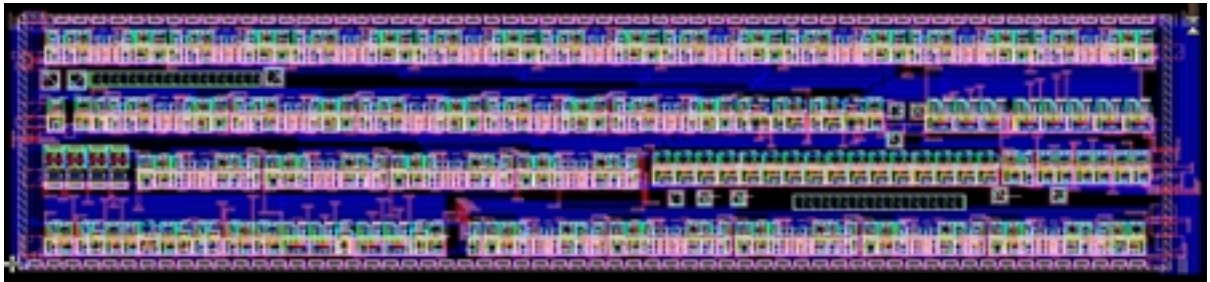Fig. 11: Digital block output waveforms after adding delay blocks.

Fig. 12: Digital block layout.

The Output Drivers

The new STIM-2 design is based on dual ±5V supplies as was the old one. Its logic circuitry is tied between the +5V and GND lines, and the –5V supply is used only for cathodic stimulation. The INTERESTIM1 power supply block generates +10V output, which is divided by two and buffered by a high current class AB unity-gain amplifier. The internal 10V, 5V and GND power lines are assumed as +5V, GND and –5V supplies, respectively, by STIM-2, which should not have any other electrical connection with the interface chip substrate. This means the interface chip digital output

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signals have to switch between +10V and +5V to be assumed as +5V and GND by STIM-2.
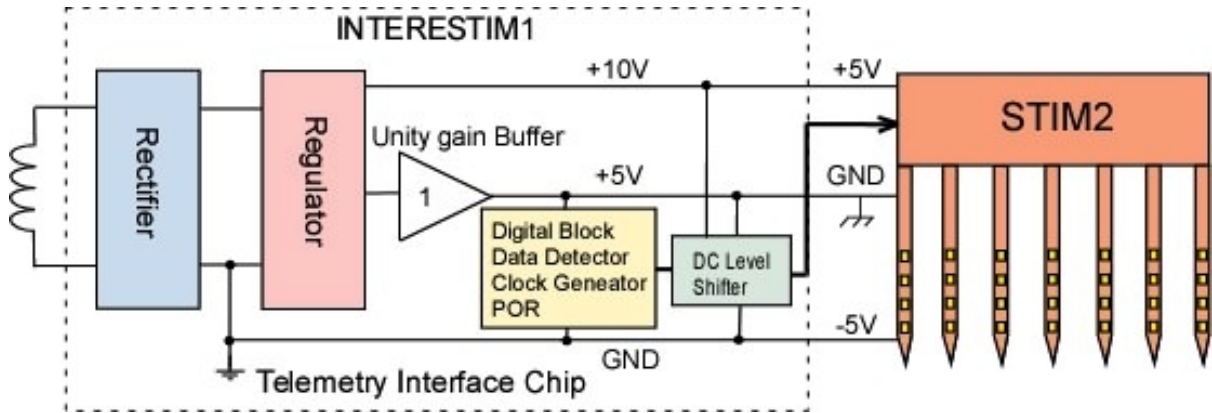

Fig. 13: Power line distribution and signal levels between INTERESTIM1 and STIM-2

There are three options for supplying the INTERESTIM1 internal circuitry:

1- (High: VDD = 10V <> Low: GND = 0V) This choice increases the dynamic power consumption significantly, which is proportional to VDD squared.

2- (High: VDD = 10V <> Low: GND = 5V) Since most of the STIM-2 power is taken from positive supply and its negative supply is only used for cathodic phase stimulation, this makes the power supply block loading highly asymmetrical which in turn causes higher output ripple; furthermore, positive output voltage drops by increasing the GND output voltage. Another disadvantage of this option is dissipation of the same amount of power taken from the positive supply in negative supply because the same current passes through unity gain buffer current sinking transistors and returns back to the internal GND.

3- (High: VDD = 5V <> Low: GND = 0V) This is the best option because the internal circuitry power taken from the negative supply balances the STIM-2 power consumption from positive supply. In the ideal case, where the interface power consumption is very close to STIM-2 power consumption, this choice can save up to 50% of the total wireless system power consumption because basically the same current passes through STIM-2 and INTERESTIM1 circuits and no extra power is dissipated in the unity gain buffer.

The third method was chosen for supplying the INTERESTIM1 internal circuitry due to its advantages over the other two methods. Figure 13 shows power line distribution and signal levels between INTERESTIM1 and STIM-2. The internal logic levels are 5V for "High" and 0V for "Low" but these levels need to be shifted to 10V for 'High" and 5V for "Low" to be compatible with STIM-2. A two-step digital level shifter was designed for this purpose, which is shown in Fig. 14.

The first two inverters buffer the input signal and generate 0-5V logic outputs. A cross-coupled differential pair, which is supplied by 10V line provides the first logic level shift from 0-5V to 0-10V and a 10V supplied inverter buffers the 0-10V output signal. Finally, the last two inverters, whose supplies are tied to the 10V and 5V power lines, perform the second level shift from 0-10V to 5-10V logic. The nice thing about this circuit is that its static power consumption is zero, and to keep the dynamic power consumption low, low W/L ratio transistors are used in the second stage. Table 1 summarizes the signal levels in 2-step level shifter circuit, and Fig. 15 shows simulated output waveforms and dynamic currents.
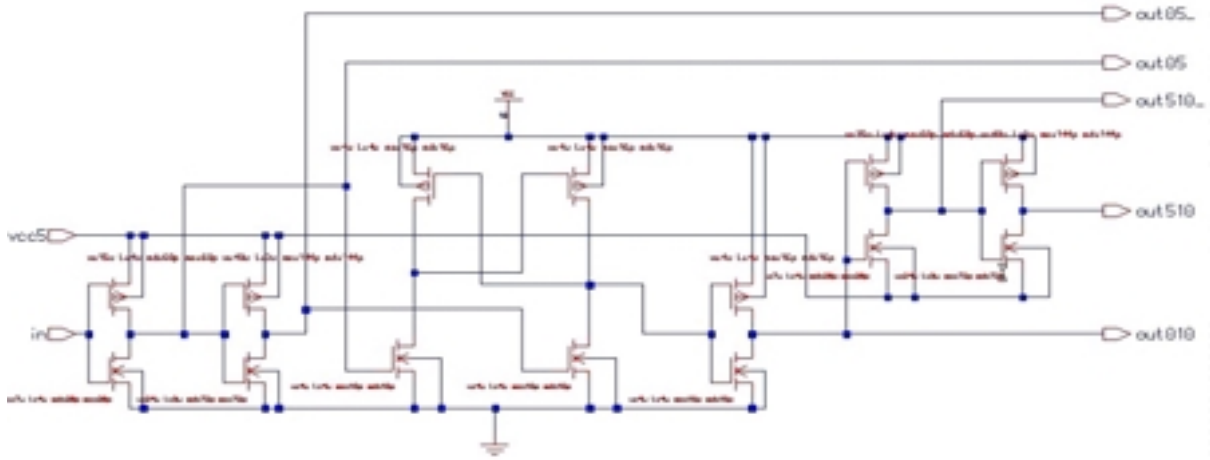

Fig. 14: Two-step digital level shifter schematic diagram for 0-5V to 5-10V logic conversion.

Table 1: Two-step digital level shifter logic

Logic Value	Out05	Out010	Out510
High	5V	10V	10V
Low	0V	0V	5V

In the layout of Fig. 16, these three stages are isolated by deep boron diffusions and several substrate, n-epi and well contacts are added to prevent latch-up.

Clock Generator

A problem observed in the clock generator block is shown in Fig. 17. The clock generator looses track of the carrier signal when its amplitude changes due to Amplitude Shift Keying. This problem can be addressed by looking at the clock generator schematic diagram in Fig. 18. Capacitors C1 and C2 divide the rectified carrier input voltage as well as high pass filter it to remove its dc baseline. The dc baseline is readjusted at threshold level of the 3-inverter ring oscillator because of the feedback provided by R1. This baseline voltage, which is altered by the carrier signal, forces the ring oscillator to

follow carrier frequency instead of its natural oscillation frequency. This is shown in Fig. 17 lower trace, which shows Ring input node and clk2, the ring oscillator output. Whenever the carrier amplitude goes through an abrupt change, the high frequency component of Ring input moves it away from the inverter threshold voltage and the oscillator stops oscillation. To solve this problem:
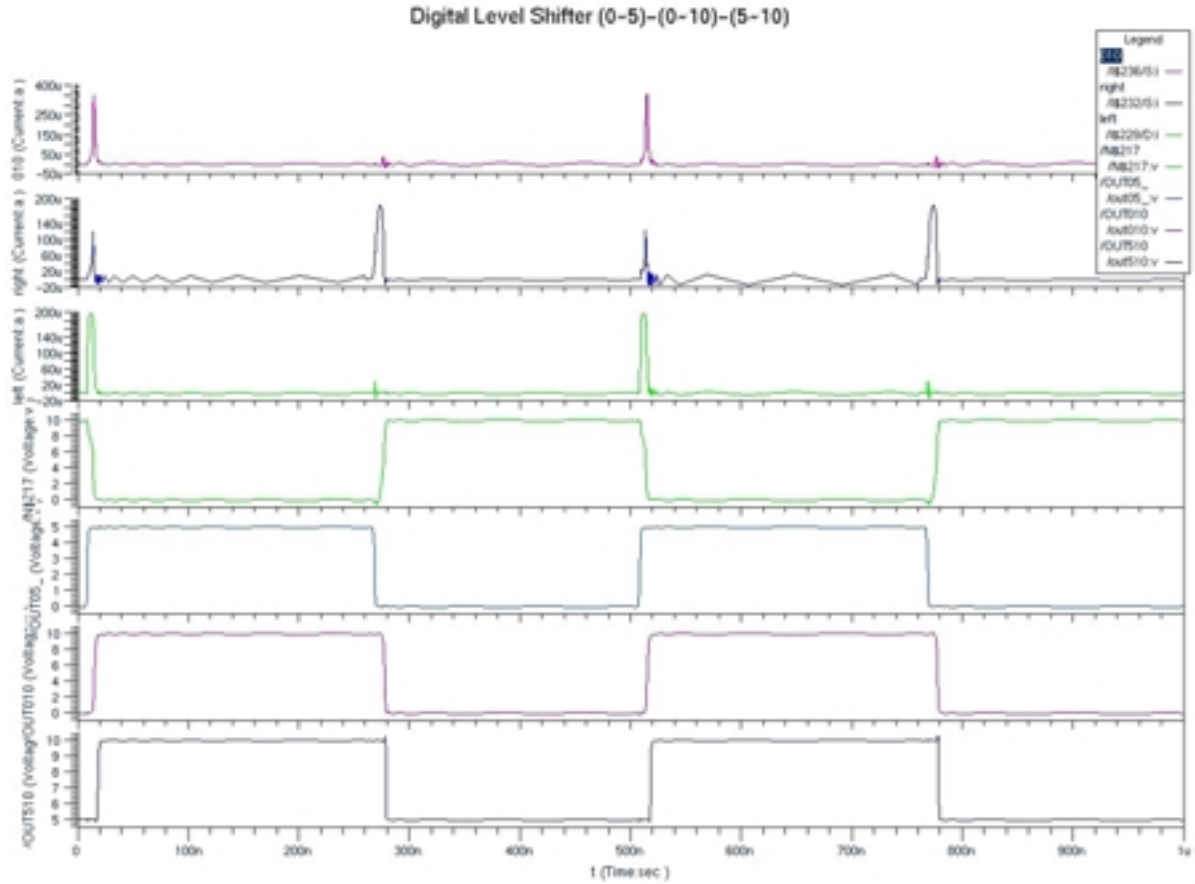

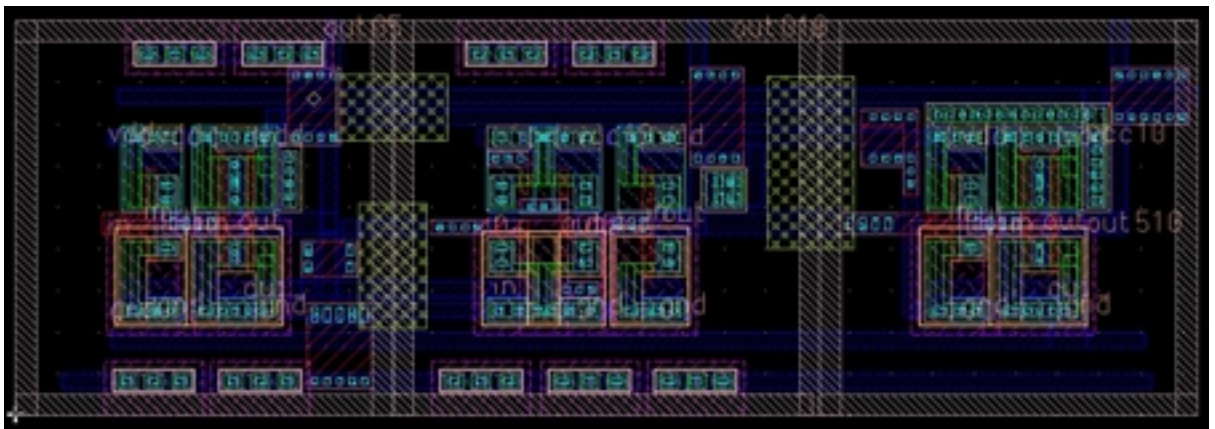Fig. 15: Two-step digital level shifter simulation waveforms

Fig. 16: Two-step digital level shifter/output driver

1- The ring oscillator feedback was strengthened by reducing R1
2- The ring oscillator self oscillating frequency was adjusted to be as close as possible to the carrier frequency by changing C3. So the ring oscillator can generate the right clock cycles even when it has lost its input.
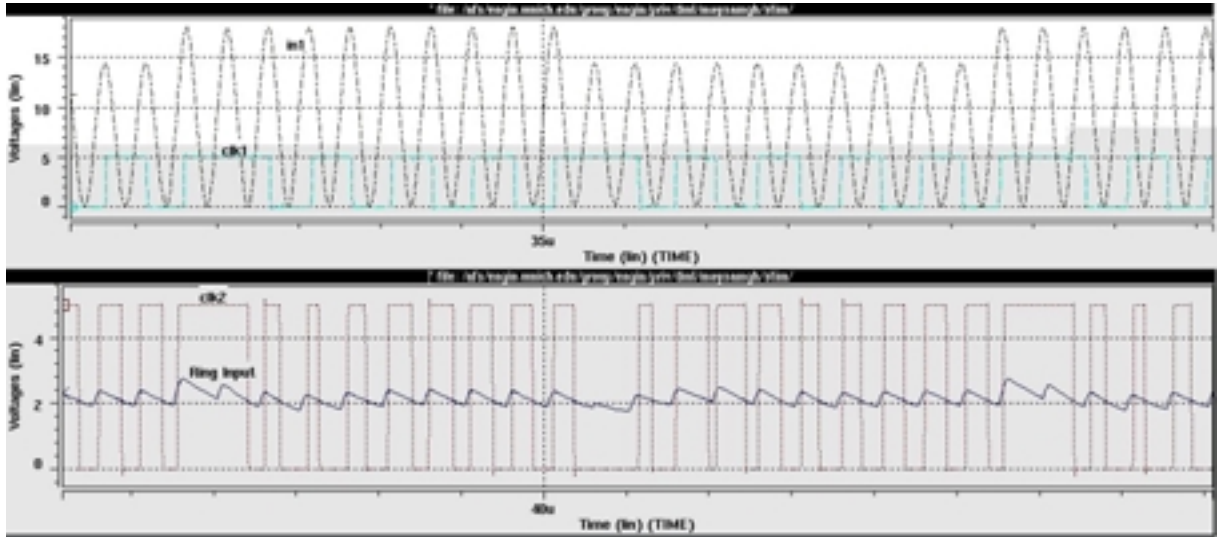3- Cutting links was provided in the layout to adjust R1 and C3 after fabrication.

Fig. 17: The clock generator looses track of the carrier signal when its amplitude changes.
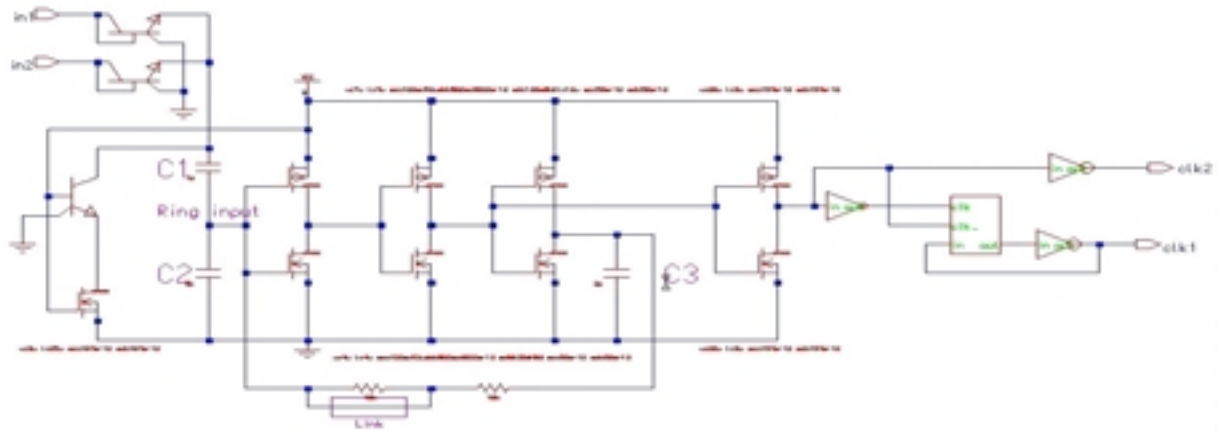

Fig. 18: Clock Generator schematic diagram.

Figure 19 shows various clock generator waveforms after fixing the problem. Now the ring oscillator continues oscillating up to 50% carrier modulation index at the input, which is more than the maximum allowable modulation for this application.

Data Detector

Several ASK demodulators were designed and simulated in order to achieve a full CMOS version of the data detector block, because of large area needed for demodulator BJTs and their risk of leakage. But none of these designs could reach the present BiCMOS demodulator baud rate and robustness when changing the carrier amplitude and modulation index. So we decided to use the BiCMOS version in INTERESTIM1 with some optimizations and room for adjustments in its new layout. Meanwhile we will continue looking for more efficient data transfer methods and full CMOS demodulator circuits. Figure 20 shows a sample data detector simulation waveform with 250Kbit/s baud rate. Robustness of this design was tested through several simulations while considering the effects of various noise and parasitic components. Figure 21 shows the data detector waveforms with 100mV ripple on its Vdd.
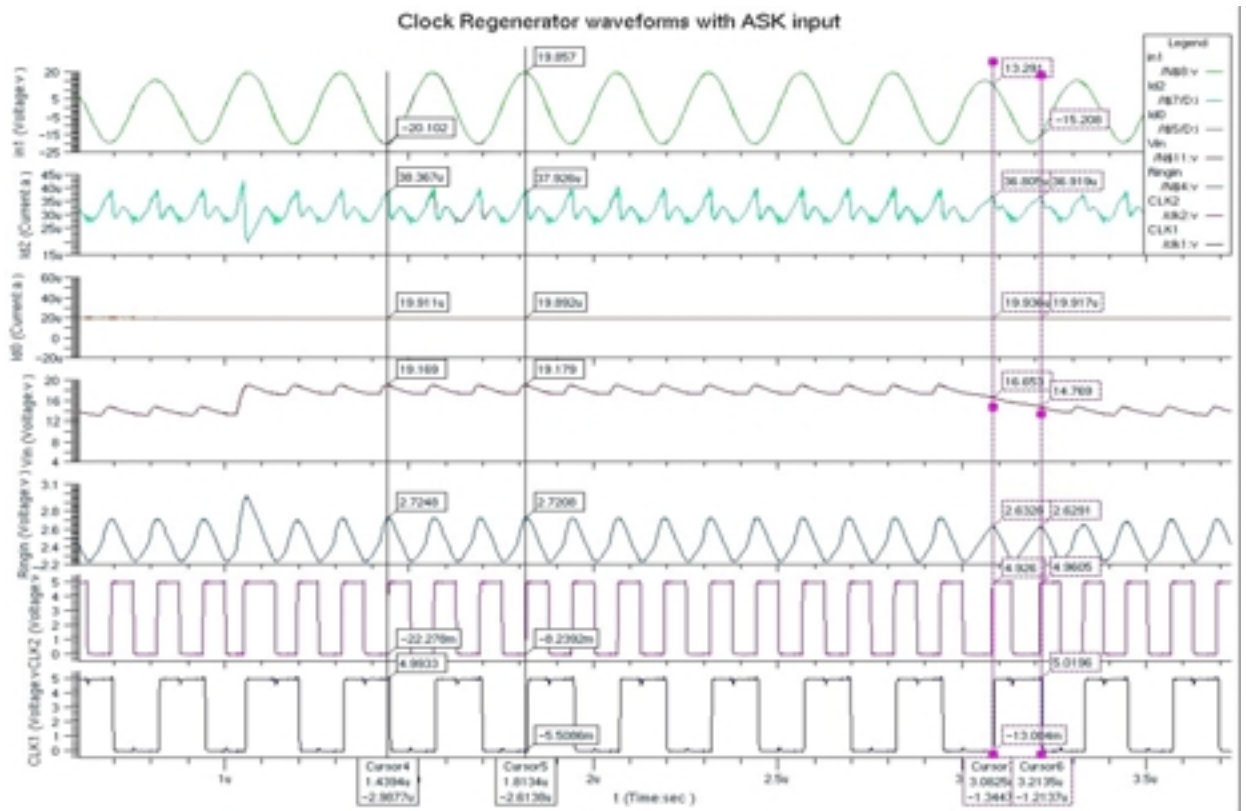

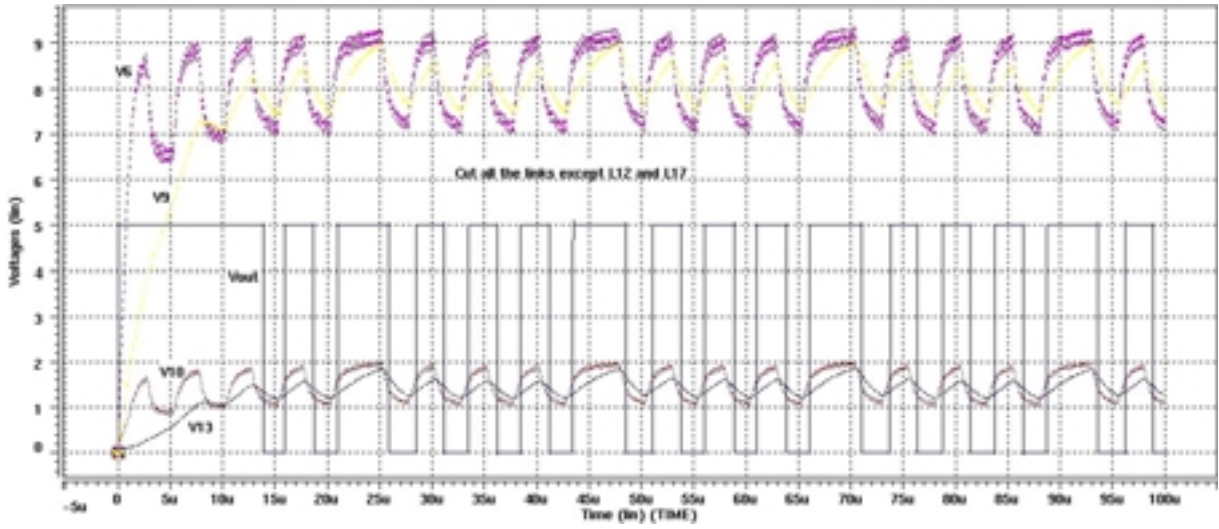Fig. 19: Clock generator waveforms with 30% modulated ASK input.

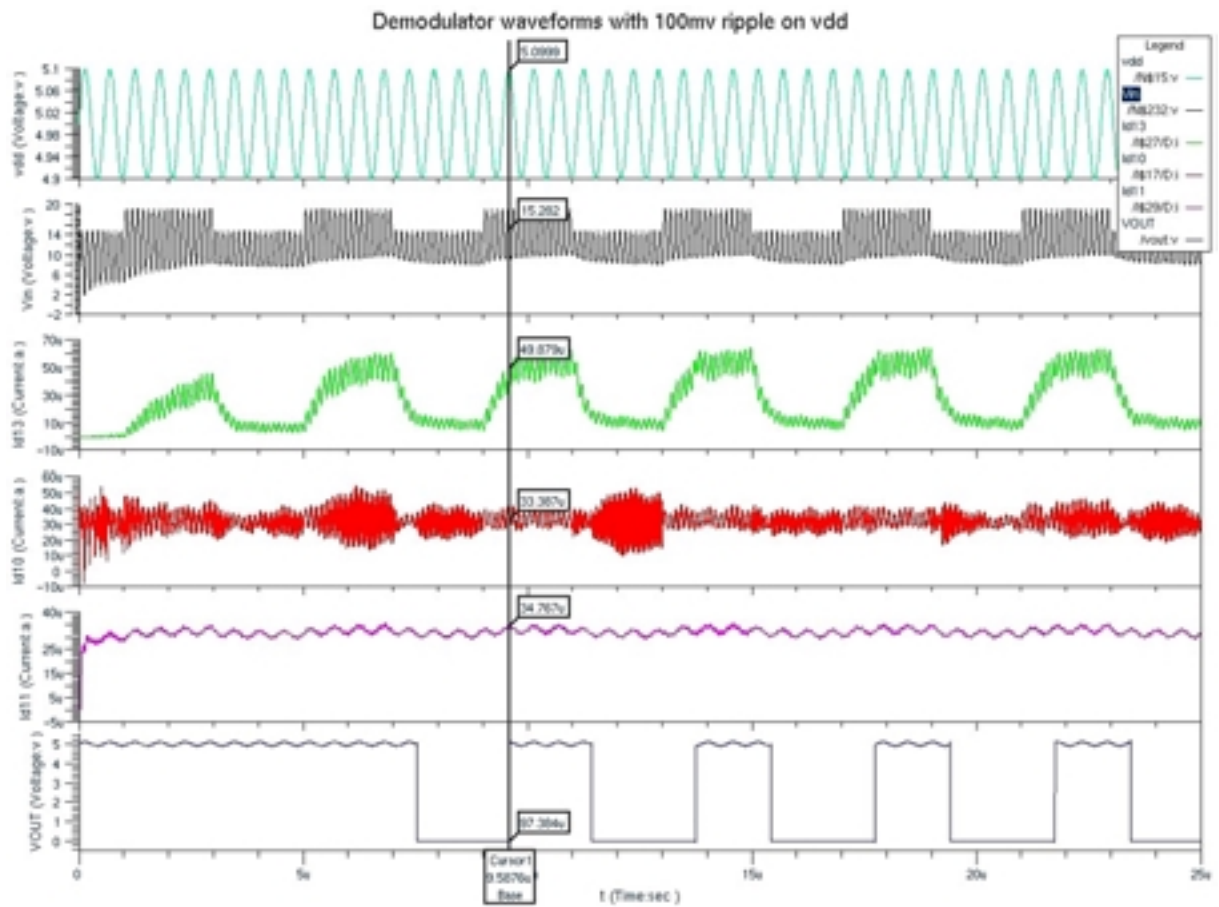Fig. 20: Data detector simulated waveforms with 250Kbit/s baud rate.

Fig. 21: Data detector waveforms with 100mV ripple on its Vdd

Fig. 22: Various on-chip rectifier designs

Rectifier Block

A variety of on-chip rectifier designs with different voltage and current handling capabilities have been simulated and laid out on a test chip for the next round of fabrication. The importance of proper on-chip rectifier design is mostly because of the leakage problem we saw in our previous designs because of the parasitic transistors that are associated with rectifying diodes. Significant increase in system power consumption and latch up are among the many problems that this leakage current can cause. Judging the superiority of one of these designs over the others based on simulations is difficult and inaccurate because there are a lot of phenomena involved in rectifying in the MHz frequency range, some of which cannot be accurately included in models. So we will actually rely on our experimental results to choose the best configuration out of these rectifier designs, which are shown in Fig. 22 schematically. Their layouts can be seen in Fig. 23.

Fig. 23: Rectifier test-chip

All diodes are basically isolated NPN transistors formed between active-P-well/N-epi layers in a BiCMOS process with their base terminal shorted to collector. Each NPN has a parasitic PNP associated with it, formed by Pwell-Nepi-Psub. These PNP transistors are shown as diodes with dashed line and can affect the functionality of the rectifier circuit.

Design A is a simple half-wave rectifier. This diode can be any one of active-Pwell, Pwell-Nepi or Nepi-Psub diodes and we have one of each on the test chip. Design C is a normal four-diode full bridge rectifier and design E is the same bridge with two diodes in series in each branch to have higher reverse break down voltage in expense of more forward voltage drop. Design B is a 2-diode full bridge rectifier taking the advantage of Psub-Nepi parasitic diodes in current return path and design D is the same thing with two diodes in series.
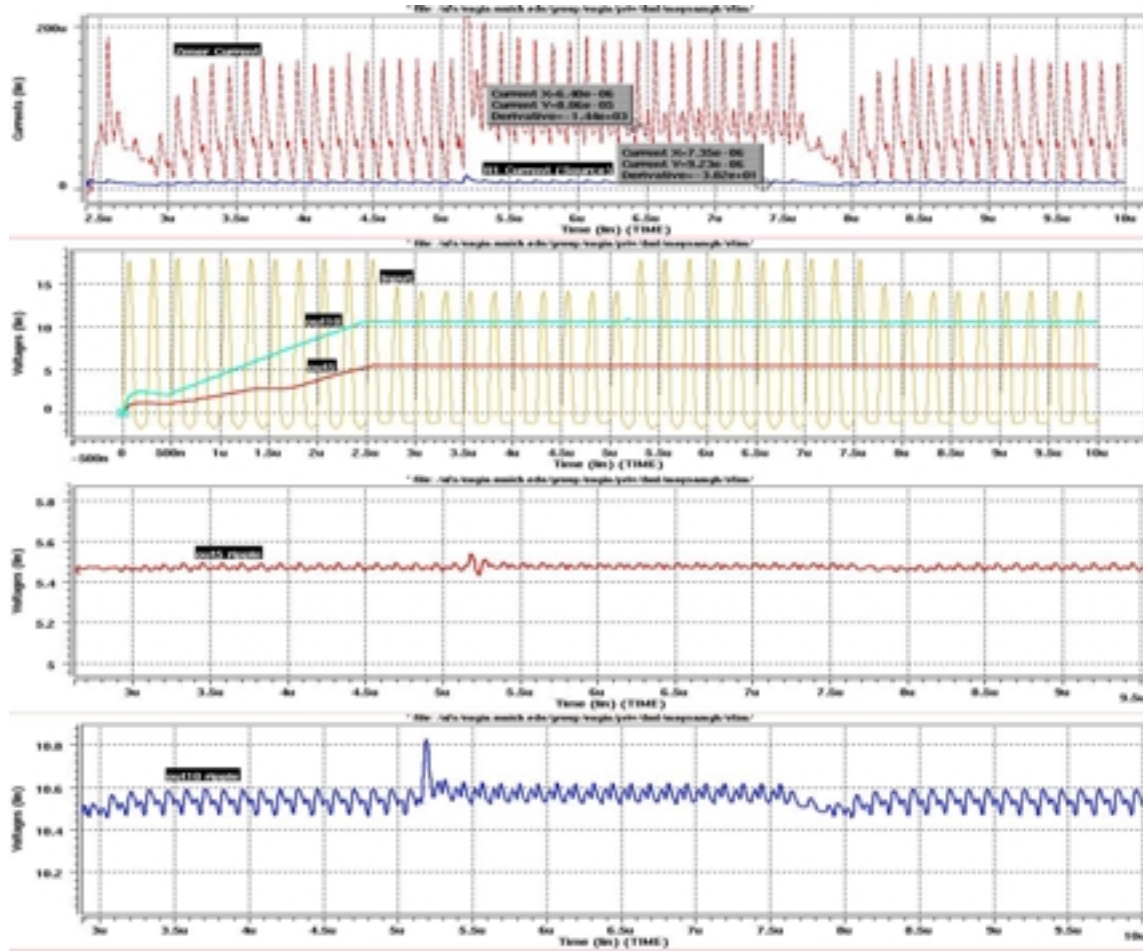

Fig. 24: Open-loop regulator (65) input and output waveforms

One of the parameters that becomes important in rectifying the carrier high frequency signal is the diode storage delay time. Two different sizes of rectifier diodes

are laid out in the Fig. 23 test-chip to see the effects of the parasitic junction capacitors and diodes on switching speed versus their current handling capability before the parasitic PNPs turn on.

Regulator Block

Two designs are being tested by the next run. The goal is to achieve a high current output with smaller values of ripple and output voltage drop. The first design, Regulator65, is an open-loop regulator based on a Zener diode voltage reference. It is similar to our previous regulator chip with many of its problems fixed.
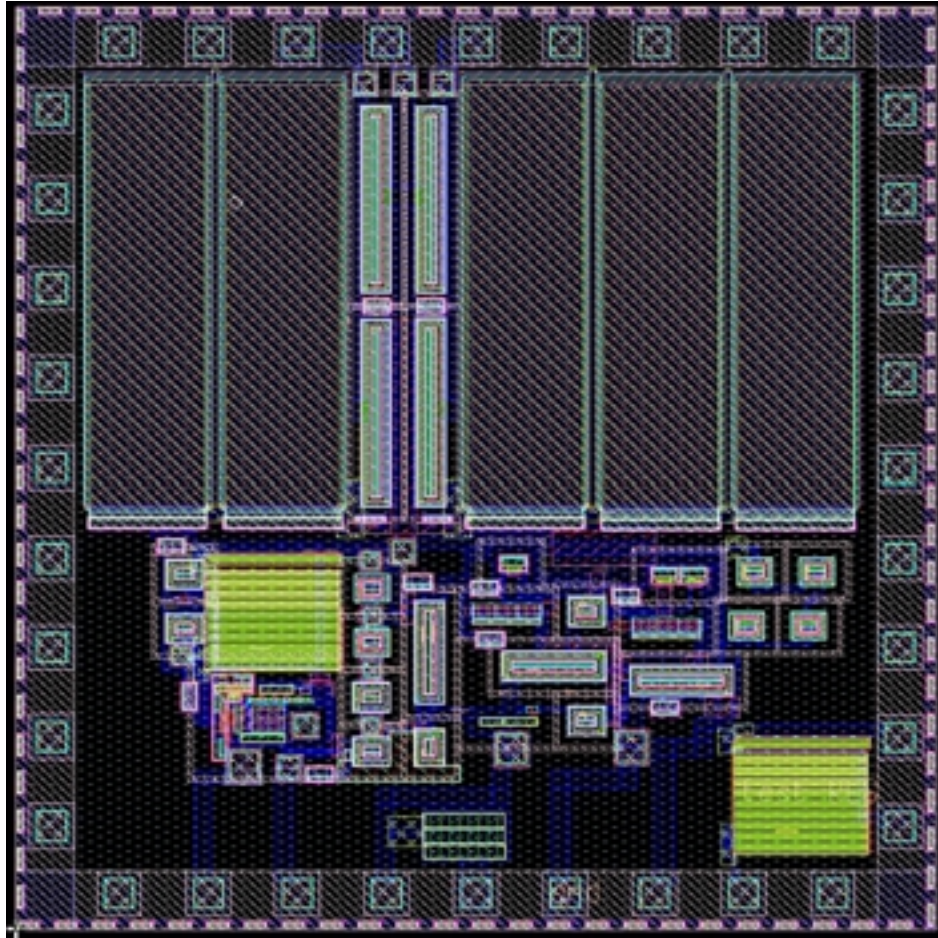

Fig. 25: The Regulator65 test-chip

Input and output voltage and current waveforms are shown in Fig. 26 with 1Kohm loads connected between 10V-5V and 5V-GND outputs. The upper trace shows the current passing through the reference Zener diode, which average basically shows the regulator power consumption. The lower traces show the ASK-modulated rectified input as well as 10V and 5V outputs with their ripples, which do not change significantly with modulation. Figure 25 shows the Regulator65 test-chip.
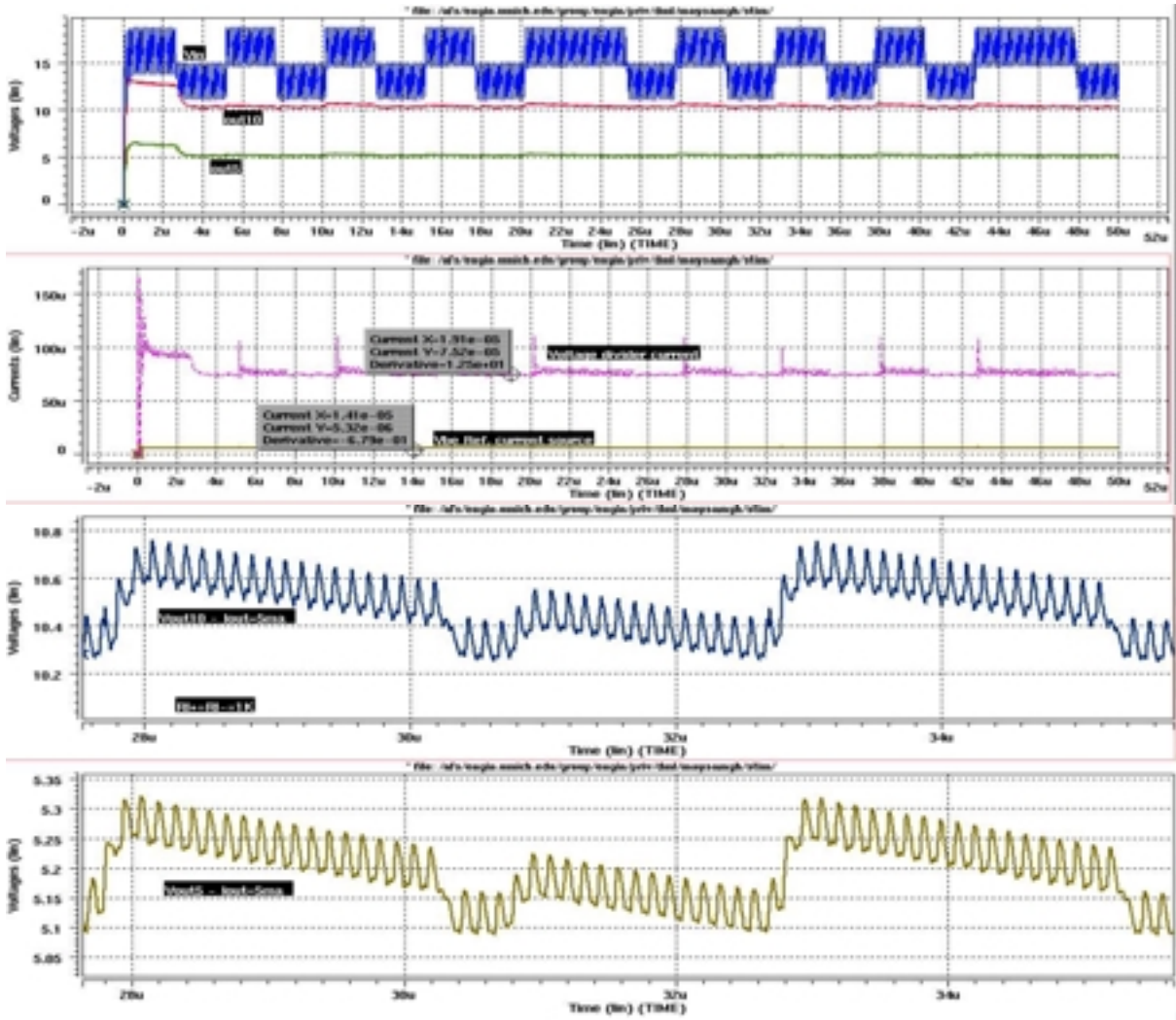
Fig. 26: Closed-loop regulator (42) input and output waveforms

The second design, Regulator42, is a closed-loop series regulator based on a V_{be} voltage reference, which is compared with a portion of the output voltage. The Regulator42 test-chip is shown in Fig. 27. The resistive output voltage divider is duplicated in the chip to be measured separately.
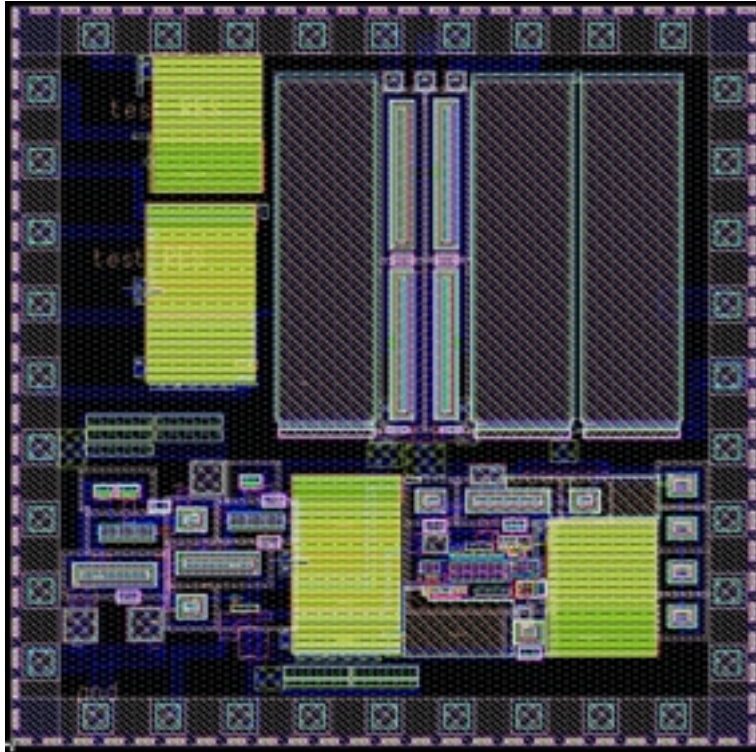
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Fig. 27: The Regulator42 test-chip

The Complete Layout

Three versions of the telemetry interface chip, INTRESTIM1, were finalized for fabrication. Figure 28 shows one of these layouts, which contains Regulator65 and the rest of blocks described above.
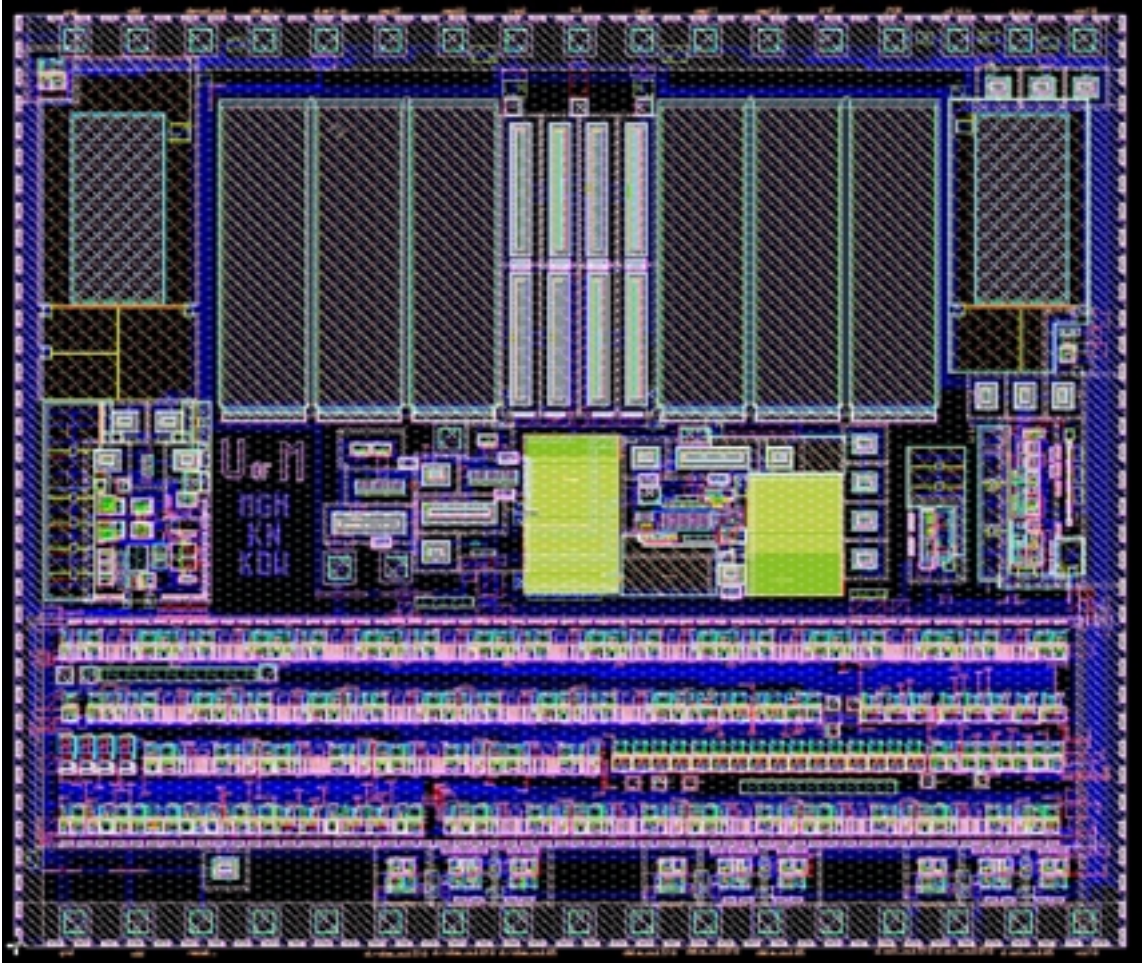
Fig. 28: INTERESTIM1 layout.

4. Conclusions

During the past quarter, work under this program focused in two areas: completion of the design of our high-end stimulating probes, STIM-2 and STIM-3, and completion of the design of a wireless interface for use with the probes. Both of these were completed and both the probes and the interface are in fabrication.

The STIM-2 and STIM-3 probes are designed to provide 64 sites and 8 parallel channels per probe. The are designed for fabrication in the U-M 3μm micromachined p-well double-poly single-metal CMOS process and operate from ±5V supplies using seven input leads. A platform chip with a layout area of about 1.1mm by 2.7mm has also been completed to allow addressing of single probes in a multi-probe 3D array. The probes produce stimulating currents over a range from –127μA to +127μA with a current resolution of ±1μA. The circuit area measures 5.8mm wide by 2.5mm wide and is designed to lay flat against the cortex to minimize vertical height of the implant. The 90° fold-over with respect to the penetrating shanks is facilitated using silicon ribbon cables.

The probe offers eight shanks on 400μm centers with eight sites per shank on 200μm centers. Any site on the probe can be used for recording using an on-chip recording amplifier having a midband gain of 40dB, a bandwidth from 3.2Hz to 14kHz, a power dissipation of 212μW, and an input-referred noise of 7.9μV/rt-Hz.

A wireless interface for use with the probes has also been developed. Many aspects of this chip have been reported previously. The complete design is now in fabrication using the U-M CMOS process. The wireless chip will be platform-mounted and we hope to demonstrate fully-wireless operation of the stimulating system before the end of the year.